**🔌 J-Link to Infineon XC164 OCDS (JTAG) Wiring**

The **XC164-32F** supports **OCDS (On-Chip Debug Support) via JTAG**. The relevant pins are on **Port 3** + TRST.

**JTAG Signals (from datasheet [XC164-32F])**

* **TCK** → P3.7
* **TMS** → P3.4
* **TDI** → P3.3
* **TDO** → P3.6
* **TRST** → Pin 36 (dedicated Test Reset)
* **RESET** → Pin 1 (RSTIN)
* **Vref** → Any **VDDP** pin (typically +5.0 V for pads)
* **GND** → Any **VSSP/VSSI** pin

**J-Link 20-pin ARM-style Header ↔ XC164 Pins**

| **J-Link Pin** | **Signal** | **XC164 Pin** | **Notes** |
| --- | --- | --- | --- |
| 1 | Vref | VDDP (e.g., Pin 9/17/38/61/87) | Must match target I/O voltage (5V on XC164). |
| 4 | GND | VSSP/VSSI (e.g., Pin 8/16/37/62/88/34/98) | Tie multiple grounds if possible. |
| 7 | TMS | P3.4 | 4.7 kΩ pull-up to Vref. |
| 9 | TCK | P3.7 | 33 Ω series resistor close to MCU (optional, for signal integrity). |
| 5 | TDI | P3.3 | 4.7 kΩ pull-up to Vref. |
| 13 | TDO | P3.6 | Connect directly; 33 Ω series resistor optional. |
| 3 | nTRST | Pin 36 (TRST) | Pull-down 4.7 kΩ to GND when not in use. |
| 15 | nRESET | Pin 1 (RSTIN) | 4.7 kΩ pull-up to Vref, J-Link can drive low. |
| 2, 6, 8, etc. | GND | Tie to ground plane | Keep short, wide. |

*(Other J-Link pins are NC for this setup.)*

**✅ Checklist for Clean Reads (XC164 via J-Link)**

1. **Target Power & VTref**
   * Provide stable **+5.0 V** to VDDP (pad supply).
   * Tie **Vref (J-Link pin 1)** to the board’s VDDP.
   * Ensure decoupling caps are close to MCU (0.1 µF + 10 µF).
2. **Pull-ups / Pull-downs**
   * **TMS, TDI** → 4.7 kΩ pull-ups to Vref.
   * **TRST** → 4.7 kΩ pull-down to GND.
   * **RESET (RSTIN)** → 4.7 kΩ pull-up to Vref.
3. **Series resistors (optional, for clean edges)**
   * Place **~33 Ω** in series with **TCK** and **TDO** near the MCU if ringing occurs on long wires.
4. **Reset Strategy**
   * Use J-Link **nRESET control** to hold MCU in reset during connect.
   * Some Infineon tools require “Connect under reset” to bypass watchdogs.
5. **OCDS Enable**
   * TRST must be held HIGH (via J-Link) to activate OCDS.
   * If TRST is tied low on your board → you’ll need to isolate/cut jumper so J-Link can drive it.
6. **Clock**
   * Ensure XTAL/oscillator is running (or drive XTAL1 with external clock if oscillator not populated).
   * Without a valid CPU clock, JTAG will not respond.
7. **Connection Settings**
   * In J-Flash or MemTool, select **C166/XC166 family**.
   * Use “5.0 V target I/O” setting.
   * Try “Connect under reset” first if normal attach fails.
8. **Verification**
   * First run a **blank check** (if protection is disabled, it will report).
   * Then dump flash to .bin → read twice, compare CRC/MD5.

⚡ With this wiring and checklist, We’ll have the best shot at pulling the firmware cleanly via JTAG before we resort to socket extraction/programmer.